REMARKS

In the Office Action the Examiner noted that claims 12, 14-16, 22, 24 and 25 are pending in the application, and the Examiner rejected all claims. The Examiner's rejections are traversed below, and reconsideration of all rejected claims is respectfully requested.

Claim Rejections Under 35 USC §103

In item 3 on pages 2-4 the Examiner rejected claims 12 and 14 under 35 U.S.C. §103(a) as being unpatentable over U.S. Patent No. 5,904,508, issued to Codama et al. (hereinafter referred to as "Codama") in view of U.S. Patent No. 5,568,288, issued to Yamazaki et al. (hereinafter referred to as "Yamazaki '288") / U.S. Patent No. 5,897,344, issued to Teramoto et al. (hereinafter referred to as "Teramoto"). The Applicants respectfully traverse these rejections.

Claim 12 of the present application recites:

> A thin film transistor (TFT), comprising:
> a substrate;
> a semiconductor layer formed over said substrate having end portions;
> a first insulating layer disposed on said semiconductor layer so as to expose ones of the end portions of said semiconductor layer;
> a gate electrode formed over said first insulating layer;
> a capping layer formed over said gate electrode;
> spacers formed over said first insulating layer and on both sidewall portions of said gate electrode and said capping layer;
> high-density source and drain regions formed at the ones of the end portions of said semiconductor layer exposed beyond said spacers, the high-density source and drain regions spaced apart from the gate electrode and the capping layer;
> low-density source and drain regions having a same conductivity as said high-density source and drain regions formed at regions of said semiconductor layer under said spacers between the gate electrode and the high-density source and drain regions, wherein said semiconductor layer has lightly doped drain (LDD) regions under said spacers; and
> source and drain electrodes which directly contact, respectively, and without contact holes, said high density source and drain regions.

Therefore, the TFT recited in claim 12 features "a capping layer formed over said gate electrode," and "spacers formed over said first insulating layer and on both sidewall portions of said gate electrode and said capping layer." The Applicants respectfully submit that the spacers formed in this manner are not disclosed in any of the cited references, either alone or in combination.

Codama discloses a TFT in which a dummy gate region 108 is used during the formation of the semiconductor layers, the dummy electrode being 108 removed after the doping which

produces the lightly doped regions 201 and the more heavily doped source and drain regions 118, 119 of the semiconductor layer (Figures 1A-3A). The dummy gate region 108 is then removed and replaced with an aluminum film 122 which will serve as the gate electrode 123 (Figures 3C-3D). In this way, aluminum may be used as the gate electrode material, even though the melting point of aluminum is too low for the temperature applied to produce the source and drain regions 118, 119. However, while spacers 113 are used to shield the lightly doped regions 201 while forming the source and drain regions 118,119, there is no capping layer formed over the gate electrode, and therefore the spacers are not formed on the sidewall portions of a capping layer. The Examiner has identified the silicon oxide film used as an interlayer dielectric film 129 in the TFT of Codama as a capping layer, but it is clearly not "a capping layer formed over said gate electrode," as recited in claim 12 of the present application. As a matter of fact, the interlayer dielectric film is formed over the entire TFT, except for the contact holes which allow the source and drain electrodes 131, 132 to contact the source and drain regions 118, 119 (Figures 4A-4D). Even if the interlayer dielectric film 129 were to be considered a capping layer, and the Applicants respectfully submit that it cannot be regarded as such, the spacers 112 are not formed on sidewall portions of the interlayer dielectric film 129, for at least two reasons. Firstly, as the aluminum film 122 covers the entire surface of the spacers 112, the spacers 112 are not in contact with the interlayer dielectric film 129 at all. Secondly, as the interlayer dielectric film 129 is formed over the entirety of the TFT, and therefore over the entirety of the spacers 112, there would be no sidewalls of the interlayer dielectric film 129 to contact even if the spacers 112 were not entirely covered with the aluminum film 122. Therefore, Codama does not disclose "spacers formed over said first insulating layer and on both sidewall portions of said gate electrode and said capping layer," as recited in claim 12 of the present application.

Similarly, Yamazaki '288 does not disclose "spacers formed over said first insulating layer and on both sidewall portions of said gate electrode and said capping layer." As a matter of fact, Yamazaki '288 does not disclose spacers at all. Figures 22(A) through 22(G) illustrate the formation of a TFT in which an insulating film 106, which serves as a capping layer, is formed on a gate electrode 107, and then an anodic oxidation film 100 is formed on the exposed portions of the gate electrode 107. This anodic oxidation film 100 cannot be considered a spacer, as is evident by Figures 22(D) through 22(G), which show that the anodic oxidation film 100 has no effect on the boundaries of the source and drain regions which result from doping the semiconductor layer with boron. Further, even if the anodic oxidation film 100 could be considered a spacer, and the Applicants respectfully submit that it clearly is not, the anodic

oxidation film 100 is not formed on the sidewall portions of the insulating film 106. Therefore, like Codama, Yamazaki '288 does not disclose "spacers formed over said first insulating layer and on both sidewall portions of said gate electrode and said capping layer."

Teramoto also does not discose "spacers formed over said first insulating layer and on both sidewall portions of said gate electrode and said capping layer." Figure 1D does disclose triangular insulators 22 with determine the positions at which electrodes 23 and 24 are in contact with source and drain regions 17 and 19 (Column 2, Lines 57-61), and these triangular insulators 22 can be characterized as spacers. But, as there is no capping layer formed over the gate electrode 15, the spacers then cannot be formed on the sidewall portions of the capping layer. Further, the spacers are not formed the gate electrode 15, but rather on the oxide layer 16 that is formed on the gate electrode 15. Even if the oxide layer 16 formed on the gate electrode 15 were to be assumed to part of the gate electrode 15, the spacers are obviously not formed on any sidewall portions of any capping layer. Therefore, like Codama and Yamazaki '288, Teramoto does not disclose "spacers formed over said first insulating layer and on both sidewall portions of said gate electrode and said capping layer."

Therefore, none of the cited references, either taken alone or in combination, disclose "spacers formed over said first insulating layer and on both sidewall portions of said gate electrode and said capping layer." As the features of claim 12 are not disclosed by the combination of the cited references, and the omitted features are not ones that would be considered as obvious by one skilled in the art, the Applicants respectfully submit that, for at least these reasons, claim 12 of the present application patentably distinguishes over the cited references, and further respectfully requests the withdrawal of the §103(a) rejection.

Further, even if the references did combine to disclose all of the features of claim 12 of the present application, and the Applicants respectfully submit that they do not, there is no motivation to combine the disclosure of Codama with either Yamazaki '288 or Teramoto. The Examiner acknowledges that Codama does not disclose "source and drain electrodes contacting high density source and drain regions without contact holes," but that this feature is disclosed in Yamazaki '288 and Teramoto. The Examiner then states that "[s]ince Codama and Yamazaki '288/Teramoto are all from the same field of endeavor, thin film transistors, Yamazaki '288's/Teramoto's teachings would have been recognized in the pertinent art of Codama," and that it would have been obvious to one skilled in the art at the time the invention was made to incorporate Yamazaki's/Teramoto's '288 teachings with the device disclosed by Codama. The Applicants respectfully submit that not only would it not have been obvious to combine the cited

references, but Codama actually teaches away from the disclosures of Yamazaki '288 and Teramoto.

MPEP § 2142 states that "[w]hen the motivation to combine the teachings of the references is not immediately apparent, it is the duty of the Examiner to explain why the combination of the teachings is proper." Here, the Examiner has simply stated, with no evidence to support the assertion, that "it would have been obvious....to combine Yamazaki '288's teachings with Codama's device since that would prevent flickering and display failure as taught by Yamazaki '288," and "it would have been obvious to incorporate Teramoto's teachings since that would minimize source/drain sheet resistance and eliminate the need for performing mask alignment as taught by Teramoto." However, one of the features of claim 12 of the present application that is lacking in Codama, namely the "source and drain electrodes which directly contact, respectively, and without contact holes, said high density source and drain regions," is not the source of the prevention of flickering and display failure, and therefore there would be no motivation to incorporate those elements into the disclosure of Codama. Yamazaki '288 discloses a method of compensating for the variation in TFT characteristics by inputting a reference signal repeated in a certain cycle and having a signal level which varies during duration of the reference signal, performing gradation display in a digital method instead of the conventional analog method of gradation display (Column 2, Line 37 through Column 4, Line 9). "The present invention is characterized in that the clear digital gradation display is possible without changing the number of frames for re-writing the screen, by taking two kinds of driving frequencies" (Column 9, Lines 53-56). The Examiner has cited the one embodiment (Figures 21 and 22), out of several embodiments disclosed in Yamazaki '288 that accomplish this method of gradation display, which appears to show electrodes formed in contact with the source and drain regions. However, this formation of the electrodes is not the source of the method, as is evidenced by the other several embodiments which perform the method without the physical structure of Figures 21 and 22. Therefore, the Applicants respectfully submit that there is no motivation to incorporate the cited formation of Yamazaki '288 into the disclosure of Codama. Similarly, as the spacers of Teramoto and Codama are both formed by vertically etching the spacers form a silicon oxide film, there is no elimination of "the need for performing mask alignment as taught by Teramoto" which would be gained by the incorporation of Teramoto into the disclosure of Codama.

Further, as Codama discloses a method of forming a TFT with a dummy gate region to produce the source and drain regions, as opposed to the actual gate electrode used in Yamazaki '288 and Teramoto, the disclosure of Codama actually teaches away from the

disclosures of Yamazaki '288 and Teramoto. For instance, Codama lacks a capping layer formed over the gate electrode, which is disclosed in Yamazaki '288. But the capping layer of Yamazaki '288 serves to protect the gate electrode from the doping of the boron ions which forms the source and drain regions of Yamazaki '288. As the gate electrode does not exist during the formation of the source and drain regions in Codama, the disclosure of Codama teaches away from the disclosure of Yamazaki '288. Similarly, Teramoto uses the gate electrode to shield the channel layer from being doped during the formation of source and drain regions. Therefore, the disclosure of using a dummy gate electrode in Codama also teaches away from the disclosure of Teramoto.

The Examiner is required to present actual evidence and make particular findings related to the motivation to combine the teachings of the references. In re Kotzab, 55 USPQ2d 1313, 1317 (Fed. Cir. 2000); In re Dembiczak, 50 USPQ2d 1614, 1617 (Fed. Cir. 1999). Broad conclusory statements regarding the teaching of multiple references, standing alone, are not "evidence." Dembiczak, 50 USPQ2d at 1617. "'The factual inquiry whether to combine the references must be thorough and searching.'" In re Lee, 61 USPQ2d 1430, 1433 (Fed. Cir. 2002) (citing McGinley v. Franklin Sports, Inc., 60 USPQ2d 1001, 1008 (Fed. Cir. 2001)). The factual inquiry must be based on objective evidence of record, and cannot be based on subjective belief and unknown authority. Id. at 1433-34. The Examiner must explain the reasons that one of ordinary skill in the art would have been motivated to select the references and to combine them to render the claimed invention obvious. In re Rouffet, 47 USPQ2d 1453, 1459 (Fed. Cir. 1998). Thus, as pointed out in In re Lee, the record must support motivation, i.e., there must be something in the record pointing out where the recited motivation can be found. In addition, there must be some discussion on how that purported motivation or suggestion is even relevant to the reference being modified.

"Obviousness can only be established by combining or modifiying the teachings of the prior art to produce the claimed invention where there is some teaching, suggestion, or motivation to do so found either explicitly or implicitly in the references themselves or in the knowledge generally available to one of ordinary skill in the art" (MPEP 2143.01). "The mere fact that references can be combined or modified does not render the resultant combination obvious unless the prior art also suggests the desirability of the combination." In re Mills, 916 F.2d 680, 16 USPQ2d 1430 (Fed. Cir. 1990). The Applicants respectfully submit that there is no motivation to combine the references of Yamazaki '288 and Teramoto, both of which would be required to disclose at least some of the elements of claim 12 of the present application, with Codama to attempt to produce the TFT as recited in claim 12 of the present application, and

respectfully requests the withdrawal of the 103(a) rejection for at least these reasons.

Claim 14 depends from claim 12 and includes all of the features of that claim plus additional features which are not taught or suggested by the cited references. Therefore, it is respectfully submitted that claim 14 also patentably distinguishes over the cited references.

In item 4 on pages 4-6 of the Office Action the Examiner rejected claim 22 under 35 U.S.C. §103(a) as being unpatentable over U.S. Patent No. 5,837,568, issued to Yoneda et al. (hereinafter referred to as "Yoneda") in view of U.S. Patent Publication No. 2003/0207502, issued to Yamazaki et al. (hereinafter referred to as "Yamazaki '502") and Yamazaki/Teramoto.

Claim 22 of the present application recites:

> An active matrix display device, comprising:
> a substrate;
> a semiconductor layer having end portions formed over said substrate;
> a first insulating layer formed over said semiconductor layer so as to expose one of the end portions of said semiconductor layer;
> a gate electrode formed over said first insulating layer;
> a capping layer formed over said gate electrode;
> spacers formed over said first insulating layer and on side wall portions of said gate electrode and said capping layer;
> high-density source and drain regions formed at the ones of the end portions of said semiconductor layer exposed beyond said spacers;
> low-density source and drain regions having a same conductivity as said high-density source and drain regions formed at off-set regions of said semiconductor layer under said spacers so as to have said semiconductor layer with lightly doped drain (LDD) regions under said spacers;
> source and drain electrodes which directly contact, respectively, and without contact holes, said high density source and drain regions;
> a planarization layer having an opening portion which exposes a portion of one of said source and drain electrodes; and
> a pixel electrode formed on the planarization layer, the pixel electrode contacting one of the second source and drain electrodes through the opening portion.

Therefore, the active matrix display device in claim 22 of the present application recites "low-density source and drain regions having a same conductivity as said high-density source and drain regions formed at off-set regions of said semiconductor layer under said spacers so as to have said semiconductor layer with lightly doped drain (LDD) regions under said spacers." In other words, these lightly doped drain regions are formed only under the spacers of the TFT. This allows for a simplified manufacturing process of the TFT, because the spacers and capping layer are themselves used to mask the LDD regions from the doping process that produces the high-density source and drain regions of the TFT.

This is in direct contrast to Yoneda, in which the low-density source and drain regions

extend beyond the side walls 15 that the Examiner has characterized as "spacers" (Figure 12F). Figure 12F shows that the low-density regions 11L extend well beyond these side walls 15, which also results in the requirement of an extra mask to be used in the manufacturing process of the TFT disclosed in Yoneda. Because the low-density regions 11L are not confined to the area under the side walls 15, a resist layer R is used to mask the low-density regions 11L when doping the high-density layers 11S and 11D (Column 13, Lines 53-64). Therefore, unlike claim 22 of the present application, Yoneda does not disclose "low-density source and drain regions having a same conductivity as said high-density source and drain regions formed at off-set regions of said semiconductor layer under said spacers so as to have said semiconductor layer with lightly doped drain (LDD) regions under said spacers."

Further, this deficiency of Yoneda is not cured by the disclosure of Yamazaki '502. In Yamazaki '502, a first impurity region 103, which the Examiner has characterized as representing the low-density source and drain regions, is not located under the spacers 109, but rather extends out under the gate electrode 107 (Figure 1). Therefore, as in Yoneda, the "low-density source and drain regions" are not formed "under said spacers." Likewise, the deficiency of Yoneda and Yamazaki '502 is not cured by Yamazaki/Teramoto.

Therefore, none of the cited references, either alone or in combination, disclose "low-density source and drain regions having a same conductivity as said high-density source and drain regions formed at off-set regions of said semiconductor layer under said spacers so as to have said semiconductor layer with lightly doped drain (LDD) regions under said spacers." As the features of claim 22 are not disclosed by the combination of the cited references, and the omitted features are not ones that would be considered as obvious by one skilled in the art, the Applicants respectfully submit that, for at least these reasons, claim 22 of the present application patentably distinguishes over the cited references, and further respectfully requests the withdrawal of the §103(a) rejection.

Further, even if the references cited by the Examiner did in combination disclose all of the features of claim 22, and the Applicants respectfully submit that they do not, there is no motivation to combine these cited references, and at least Yamazaki '502 teaches away from the remaining cited references.

Specifically, the Examiner states that "[i]t would have been obvious to one skilled in the art at the time the invention was made to incorporate the teachings of Yamazaki '502 with Yoneda's since the spacers would function as masking layers." However, Yamazaki '502 teaches away from the thin film transistor of Yoneda, as the thin film transistor of Yamazaki '502

is formed that will emulate the operating characteristics of a MOSFET type transistor (Paragraphs [0007] through [0019]). This is accomplished by forming three differently doped regions in the semiconductor layer of the thin film transistor, along with the non-doped channel region. Along with this arrangement of differently doped regions of the semiconductor layer, the most lightly doped region of the semiconductor layer extends under the gate electrode, so that "[d]eterioration due to a hot carrier can also be effectively suppressed" (Paragraph [0019]). As the spacers 15 shown in Figure 12F of Yoneda are placed specifically to keep implanted ions out of the channel region 11N, and therefore actually extend the undoped channel region 11N outside and partially under the spacers 15, which is the opposite of the goal of Yamazaki '502, the disclosure of Yamazaki '502, for at least this reason teaches away from that of Yoneda. Similarly, as neither Yamazaki '288 nor Teramoto disclose three differently doped regions or a doped region extending under a gate electrode, but quite to the contrary maintain a non-doped region under the gate electrode, Yamazaki '502 also teaches away from Yamazaki '288 and Teramoto. Further, as discussed previously in this Response, neither the prevention of "flickering and display failure as taught by" Yamazaki '288 nor the elimination of "the need for performing mask alignment as taught by Teramoto" provide any valid motivation for combining these references with Yamazaki '502 or Yoneda.

Therefore, as there is no motivation to combine the references of Yamazaki '502 with Yoneda, nor is there any reason to combine Yamazaki '288 or Teramoto with either Yamazaki '502 or Yoneda, the Applicants respectfully submit that claim 22 of the present application patentably distinguishes over the cited references. As such, the Applicants respectfully request the withdrawal of the Examiner's §103(a) rejection.

In item 5 on pages 6-7 of the Office Action the Examiner rejected claims 15 and 16 under 35 U.S.C. §103(a) as being unpatentable over Codama in view of Yamazaki '288/Teramoto as applied to claims 12 and 22 above and further in view of Japanese Patent No. 11-261076, issued to Yamazaki et al. (hereinafter referred to as "Yamazaki '076").

As discussed previously, claim 12 patentably distinguishes over the references cited against it. Further, claims 15 and 16 depend from claim 12, and include all of the features of that claim plus additional features which are not taught or suggested by the cited references. Further, Yamazaki '076 does not cure the deficiencies of the references cited against claim 12. Therefore, it is respectfully submitted that claims 15 and 16 also patentably distinguish over the cited references.

In item 6 on page 7 of the Office Action the Examiner rejected claim 24 under 35 U.S.C.

§103(a) as being unpatentable over Yoneda in view of Yamazaki '502 and Yamazaki '288/Teramoto as applied to claim 22 above and further in view of Yamazaki '076.

As discussed previously, claim 22 patentably distinguishes over the references cited against it. Further, claim 24 depends from claim 22, and includes all of the features of that claim plus additional features which are not taught or suggested by the cited references. Further, Yamazaki '076 does not cure the deficiencies of the references cited against claim 22. Therefore, it is respectfully submitted that claim 22 also patentably distinguishes over the cited references.

Although the Office Action Summary indicates that claim 25 is rejected, the Examiner has provided no explanation in the Office Action for the rejection of claim 25. Therefore, the Applicants respectfully request that the Examiner indicate that claim 25 is accordingly allowed.

Summary

There being no further outstanding objections or rejections, it is submitted that the application is in condition for allowance. An early action to that effect is courteously solicited.

Finally, if there are any formal matters remaining after this response, the Examiner is requested to telephone the undersigned to attend to these matters.

If there are any additional fees associated with filing of this Amendment, please charge the same to our Deposit Account No. 503333.

Respectfully submitted,

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